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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/672,223 | 09/27/2000 | Yun-Sang Lee | AB-1043 US | 6183 |

7590 07/14/2003

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| EXAMINER | |
|---|---|
| WHITTINGTON, ANTHONY T | |
| ART UNIT | PAPER NUMBER |
| 2133 | |

DATE MAILED: 07/14/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/672,223 | LEE, YUN-SANG | |
| | Examiner | Art Unit | |
| | Anthony T Whittington | 2133 | |

*-- The MAILING DATE of this communication appears on th cover sheet with th correspond nce address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *29 May 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

***Response to Arguments***

Applicant's arguments filed 5-29-03 have been fully considered but they are not persuasive.

The Examiner has reconsidered the claims and concluded that the prior art of record teaches the claimed inventions as earlier presented in the first office action (See paper 8).

As per claims 1-4, the Applicant contends that Surlekar does not teach a data output buffer that transfers internal signals external to an integrated circuit device through input/output pads found in the Applicant's argument on page 7, paragraphs 2 and 3.

The Examiner disagrees and asserts that the prior art of record (Surlekar) teaches a method and integrated circuit for internal state monitoring that comprises all the elements of the instant application. Surlekar teaches a plurality of internal circuits (row and column address buffers, 11 and 12) that generates internal signals (address signals) used for addressing storage locations in Figure 1. Surlekar teaches a selection circuit (35) for controlling transfer paths of the internal signals (signals from input/output lines) and data in response to selection signals (select local input/output amplifier) in Figure 3. Surlekar teaches a data output buffer (16) for transferring the internal signals (data signals) to an outside of the device through data input/output pads (data in register and data out register, 17 and 18) in Figure 1. In column 1, lines 37-40 and column 2,lines 1-20, Surlekar refers in greater detail the transferring of internal signals via data input/output buffers in conjunction with data-in/data-out registers (data pads) to an external device (DRAM memory unit for testing). Surkelar's data input/output buffers with the data-in/data-out registers fulfills the role of the Applicant's data buffer with data pads for assisting in the transfer of internal signals to an integrated device (memory unit) by addressing

storing locations and controlling internal operations. Therefore, Surlekar meets all the claim limitations of the instant and the 102 rejections of claims 1-4 are maintained.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 5-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Surlekar (U.S. 5,668,764).

As per claims 5,9,16 and 20, Surlekar teaches internal signals that include row information, column information and control information in column 1, lines 28-34.

As per claims 6,7,10,11,14 and 18, Surlekar teaches a test information input circuit(66) that generates the selection signals and sends the selection signals to the selection circuit(67) in Figure 5.

As per claims 8,12,15 and 19, Surlekar teaches the test mode, logical states, and detecting are based on dynamic random access memory control information in column 2, lines 17-29.

As per claims 13 and 17, Surlekar teaches using the internal signals for addressing storage locations and for controlling internal operations in column 1, lines 14-42.

The previous rejection is maintained. The following is the previous rejection:

**DETAILED ACTION**

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4 are rejected under 35 U.S.C. 102(b) as being anticipated by Surlekar (U.S. 5,668,764).

As per claim 1, Surlekar teaches an integrated circuit that comprises all the elements of the instant application. Surlekar teaches a plurality of internal circuits (row and column address buffers, 11 and 12) that generates internal signals (address signals) used for addressing storage locations in Figure 1. Surlekar teaches a selection circuit (35) for controlling transfer paths of the internal signals (signals from input/output lines) and data in response to selection signals (select local input/output amplifier) in Figure 3. Surlekar teaches a data output buffer (16) for transferring the internal signals (data signals) to an outside of the device through data input/output pads (data in register and data out register, 17 and 18) in Figure 1.

As per claim 2, Surlekar teaches an integrated circuit that comprises all the elements of the instant application. Surlekar teaches a plurality of internal circuits (row and column address buffers, 11 and 12) that generates internal signals (address signals) used for addressing storage locations in Figure 1. Surlekar teaches a first selection circuit (35) for receiving the internal signals (signals from input/output lines) in response to selection signals (select local input/output amplifier) in Figure 3. Surlekar teaches a second selection circuit (multiplexer, 47) for receiving output signals from the first selection circuit (35, Figure 3) and output signals from a sense amplifier (33,Figure 3). Surlekar teaches a data output buffer (16) for transferring the internal

signals (data signals) to an outside of the device through data input/output pads (data in register and data out register, 17 and 18) in Figure 1.

As per claim 3, Surlekar teaches a method for monitoring internal signals in an integrated circuit device having input/output pads (data in register and data out register, 17 and 18, Fig.1) that comprises all the steps of the instant application. Surlekar teaches detecting a test mode in column 4, lines 34-45, which state: "In the typical operation of a DRAM memory unit... During a non-test operation cycle...bits are selected and applied to the output terminal." The determination of the operation (test mode or non-test mode) expresses that there is detection for the test mode. Surlekar teaches selecting a part of internal signals (signals from input/output lines) of the integrated circuit device in Figure 3. Surlekar teaches transferring the part of the internal signals (data signals) to an outside of the integrated circuit device through the input/output pads (data in register and data out register, 17 and 18) in Figure 1.

As per claim 4, Surlekar teaches a method for monitoring internal signals in an integrated circuit device a having sense amplifier (33, Fig. 3), a data output buffer (16, Fig.1), and input/output pads (data in register and data out register, 17 and 18, Fig. 1) comprising all the steps of the instant application. Surlekar teaches detecting a test mode in column 4, lines 34-45, which state: "In the typical operation of a DRAM memory unit... During a non-test operation cycle...bits are selected and applied to the output terminal." The determination of the operation (test mode or non-test mode) expresses that there is detection for the test mode. Surlekar teaches selecting a part of internal signals (signals from input/output lines) of the integrated circuit device in Figure 3. Surlekar teaches selecting an alternative one of transfer paths (multiplexer, 47, Fig. 5) of the part of the internal signals (expected data signal) and output signals from the

sense amplifier (33, Fig. 3). Surlekar teaches transferring the part of the internal signals (data signals) to an outside of the integrated circuit device through the data output buffer (16, Fig. 1) input/output pads (data in register and data out register, 17 and 18) in Figure 1.

***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following patents are cited to further show the state of art with respect to internal state monitoring in general:

U.S. Pat No. 6,272,588 to Johnston et al.

U.S. Pat No. 5,495,487 to Whetsel,Jr.

U.S. Pat No. 5,396,499 to Urai

U.S. Pat No. 5,463,635 to Kumazawa et al.

U.S. Pat No. 6,016,560 to Wada et al.

U.S. Pat No. 5,706,235 to Roohparvar et al.

U.S. Pat No. 4,144,536 to Ardezzone et al.

U.S. Pat No. 4,875,003 to Burke

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anthony T Whittington whose telephone number is 703-306-5617. The examiner can normally be reached on Monday-Friday 7:30a.m.-4:00p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 703-305-9595. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7239 for regular communications and 703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

A.W.
June 30, 2003

ALBERT DECADY
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